What is claimed is:

1. A method for forming a bit line of a semiconductor device, comprising the steps of:

forming I-type active regions in a minimum line width on a semiconductor substrate, the active regions being separately positioned from the adjacent active regions by a minimum line width distance;

forming word lines of a minimum line width which divide one I-type active region into three, and cross the divided I-type active regions;

forming a plug poly on the active region between the word lines;

forming an interlayer insulation film over the resultant structure;

forming a bit line contact plug to be overlapped with the plug poly by a predetermined width; and

forming a bit line of a minimum line width to be overlapped with the bit line contact plug by a predetermined width, the bit line being formed in orthogonal to the word lines and in parallel to the I-type active regions.

2. The method according to claim 1, wherein the word lines are formed by stacking a conductive layer for the word line, a tungsten silicide layer and a mask oxide film.

3. The method according to claim 2, wherein a thickness of the mask oxide film ranges from 3000 to 10,000Å.

4. The method according to claim 2, wherein a nitride film replaces the mask oxide film.

5. The method according to claim 1, wherein a thickness of the interlayer insulation film corresponds to 30 to 40% of the thickness of the mask oxide film.

6. The method according to claim 1, wherein the bit line contact plug is overlapped with the plug poly by 30 to 70%.

7. The method according to claim 1, wherein the bit line is overlapped with the bit line contact plug by 30 to 70%.

8. A semiconductor device formed on a semiconductor substrate comprising active regions, bit lines, first conductive plugs, second conductive plugs, and word lines and characterized by a minimum line width "F", and a minimum spacing width, and a cell size of less than $8F^2$ comprising:

parallel rows of active regions of minimum line width and a basic rectangular shape arranged in the semiconductor substrate with adjacent active regions being separated by the minimum spacing width;

parallel columns of word lines of minimum line width arranged in a direction perpendicular to the parallel rows of active regions with adjacent word lines being separated by the minimum spacing, the word lines being positioned to that two word lines cross each active region leaving three uncovered portions, a center portion and two end portions, in each active region;

an insulating film formed between the word lines;

first conductive plugs positioned between adjacent bits lines and contacting an uncovered portion of an active region;

an interlayer insulating film formed above the first conductive plugs;

bit line contact plugs positioned above, partially overlapping, and in contact with the first conductive plugs; and

parallel rows of bit lines of minimum line width arranged in a direction parallel to the parallel rows of active regions with adjacent bit lines being separated by the minimum spacing, the bit lines being positioned to partially overlap and contact the bit line contact plugs.

9. A method of forming DRAM cells on a semiconductor substrate, each of the DRAM cells being characterized by a minimum line width, F, and a minimum spacing, S, wherein the area of a single DRAM cell is less than $8F^2$ comprising the steps of:

forming active regions in the semiconductor substrate, the active regions being characterized by the minimum width F and a length of approximately 5F, wherein the active regions are arranged in parallel rows and separated from adjacent active regions by the minimum spacing S, and further wherein active regions in adjacent rows are offset from each other in a longitudinal direction;

forming word lines on the semiconductor substrate, each word line being characterized by the minimum width F, wherein each word line is parallel to, and separated by the minimum spacing S from, adjacent word lines, and further wherein the word lines are perpendicular to the rows of active regions;

depositing an insulating film between the word lines;

forming first openings through the insulating film to expose portions of the active regions between the word lines;

forming first conductive plugs to fill the first openings;

forming an interlayer insulating film;

forming second openings through the interlayer insulating film to expose a portion of the first conductive plugs;

forming second conductive plugs to fill the second openings and partially overlap the first conductive plugs; and

forming bit lines that partially overlap and make contact with the second conductive plugs, the bit lines being characterized by the minimum line width F, wherein adjacent bit lines are parallel and separated by the minimum spacing S, and further wherein the bit lines are oriented in a direction parallel to the rows of active regions.

10. A method according to claim 9, wherein the step of forming the word lines further comprises forming a stacked structure comprising at least three materials, the three materials being a non-metallic conductor, a metallic conductor, and an insulator.

11. A method according to claim 10, wherein the non-metallic conductor is polysilicon, the metallic conductor is tungsten silicide, and the insulator is silicon dioxide.

12. A method according to claim 10, wherein the non-

metallic conductor is polysilicon, the metallic conductor is tungsten silicide, and the insulator is silicon nitride.

13. A method according to claim 11 or 12, wherein the thickness of the insulator is between 3000 and 10,000Å.

14. A method according to claim 9, wherein the second conductive plugs overlap the first conductive plugs by between 30% and 70%.

15. A method according to claim 14, wherein the bit lines overlap the second conductive plugs by between 30% and 70%.

16. A DRAM device comprising a plurality of DRAM cells formed on a semiconductor substrate, each DRAM cell being characterized by a minimum line width, F, and a minimum spacing, S, wherein the area of a single DRAM cell is less than $8F^2$ comprising:

active regions in the semiconductor substrate, the active regions being characterized by the minimum width F and a length of at least about 5F, wherein the active regions are arranged in parallel rows and separated from adjacent active regions by the minimum spacing S, and further wherein active regions in adjacent rows are offset

from each other in a longitudinal direction;

word lines, each word line being characterized by the minimum width F, wherein each word line is parallel to, and separated by the minimum spacing S from, adjacent word lines, and further wherein the word lines are perpendicular to the rows of active regions;

an insulating film formed over the word lines;

first conductive plugs extending through the insulating film between adjacent word lines and making contact to portions of the active regions between adjacent word lines;

an interlayer insulating film formed over the first conductive plugs;

second conductive plugs extending through the interlayer insulating film, the second conductive plugs partially overlapping and contacting the first conductive plugs; and

bit lines that partially overlap and make contact with the second conductive plugs, the bit lines being characterized by the minimum line width F, wherein adjacent bit lines are parallel and separated by the minimum spacing S, and further wherein the bit lines are oriented in a direction parallel to the rows of active regions.